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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/675,801	09/29/2000	Jeffrey L. Rabe	042390.P9428	8877

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EXAMINER
PHAN, RAYMOND NGAN

ART UNIT	PAPER NUMBER
2181	6

DATE MAILED: 09/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n N .	Applicant(s)	
	09/675,801	RABE ET AL.	
	Examiner	Art Unit	
	Raymond Phan	2181	

-- The MAILING DATE of this communication appears on the c ver sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-18 and 31-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18 and 31-60* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Part III DETAILED ACTION

Notice to Applicant(s)

1. This action is responsive to the following communications: amendment filed on June 25, 2003.

2. This application has been examined. Claims 1-18 and 31-60 are pending.

Specification

3. The title of the invention is accepted.

Claim Rejections - 35 USC § 112

4. Claims 10-18 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 10 metes and bounds can not be determined and cause the claim to be vague and indefinite.

5. The remaining claims, not specifically mentioned, are rejected for incorporating the defects from the parent claim by dependency.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 1-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bennett (US No. 6,466,998) in view of Pawlowski (US No. 6,401,153).

In regard to claims 1, 7, 10, Bennett discloses method comprising the step of receiving an interrupt (see col. 5, lines 54-67); converting the interrupt into an upstream memory write interrupt (see col. 6, lines 4-45). But Bennett does not specifically disclose the converting the upstream memory write interrupt into a front side bus (FSB) interrupt transaction. However Pawlowski discloses the converting (i.e. decodeing) the upstream interrupt into a front side bus (FSB) interrupt transaction (see col. 4, lines 30-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Bennett because it would increase numbers of peripheral added to the system

In regard to claims 2, 5, 8, Pawlowski discloses wherein the interrupt is generated by a PCI device (see col. 3, lines 41-51).

In regard to claims 3, 6, 9, Pawlowski discloses wherein the FSB interrupt is received by the processor (see col. 4, lines 37-44).

In regard to claims 4, Pawlowski discloses the method comprising the step of receiving a message signaled interrupt (see col. 4, lines 37-44); forwarding the message interrupt (see col. 4, lines 37-44); converting the message interrupt into an FSB interrupt transaction (see col. 4, lines 45-64).

In regard to claim 11, Bennett discloses the chipset comprising at least one I/O controller hub (ICH), P64H, and AGP device (see figure 1).

In regard to claim 12, Bennett discloses the I/O component of an APIC configured to convert the interrupt into the upstream interrupt (see col. 4, lines 31-46).

In regard to claim 13, Bennett discloses the chipset comprising a HUB interface coupled to the first end of IOxAPIC and coupled to the second end to MCH, wherein the memory control hub configured to convert the upstream interrupt into the FSB interrupt transaction (see figure 1, col. 4, lines 4-43).

In regard to claim 14, Bennett discloses the interrupt is generated by the PCI device (see col. 4, lines 31-44) and wherein the chipset is coupled to the processor (see figure 1).

In regard to claim 15, Bennett teaches the claimed subject matter as discussed above except the teaching of message interrupt. However Pawlowski discloses receiving a message signaled interrupt (see col. 4, lines 37-44). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Bennett because it would increase numbers of peripheral added to the system.

In regard to claim 16, Bennett discloses the chipset comprising a HUB interface coupled to the first end of IOxAPIC and coupled to the second end to MCH, wherein the memory control hub configured to convert the upstream interrupt into the FSB interrupt transaction (see figure 1, col. 4, lines 4-43).

In regard to claim 17, Bennett discloses wherein the routing mechanism configured to flush the upstream interrupt before propagating an interrupt upstream (see col. 6, lines 16-43).

In regard to claim 18, Pawlowski discloses wherein the interrupt controller receive the EOI from the processor and broadcast the EOI to at least one device (see col. 6, liens 40-55).

11. Claims 31-60 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Melo et al. (US No. 6,212,590) in view of Pawlowski (US No. 6,401,153).

In regard to claims 31, 34, 37, 44, 51, 59, Melo et al. disclose the method comprising receiving, at an I/O controller, an interrupt request from an I/O device (see col. 6, lines 29-59); generating, at the I/O controller, a memory request at the predetermined address in the response the interrupt request (see col. 6, lines 29-59); transmitting the memory request to the memory, the memory request being processed at the memory controller as one or more memory cycles (see col. 6, line 39 through col. 7, line 29). But Melo et al. do not specifically disclose memory request is being routed to a coupling with one ore more processors as a part of one or more interrupt message transactions on the bus (see col. 4, lines 30-64). Therefore, it would have been obvious to a person of an ordinary skill in the art at the time the invention was made to have combined the teachings of Pawlowski within the system of Melo et al. because it would increase numbers of peripheral added to the system.

In regard to claims 32, 52, Melo et al. disclose wherein the memory request is a memory write request to the memory controller (see col. 6, lines 29-59).

In regard to claims 33, 38, 44, 53, Melo et al. disclose wherein the interrupt request is one of the interrupt request hardware signal and a memory write request to the I/O controller (see col. 6, lines 29-59).

In regard to claims 39, 46, 54, Melo et al. disclose wherein the memory request is received one or more I/O device coupled to the memory controller (see col. 6, line 29-59).

In regard to claims 40, 47, 55, Pawlowski et al. disclose wherein the interrupt is marked as lowest priority re-directable and redirected to the lowest priority register (see col. 8, lines 15-37).

In regard to claims 41, 48, 56, Pawlowski et al. disclose redirecting at least one interrupt based on the task priority information (see col. 4, lines 45-64).

In regard to claims 42, 49-50, 57-58, Pawlowski e al. disclose further comprising providing support for the updated TPR transactions to update at least one updated TPR register (see col. 9, lines 25-51).

In regard to claim 43, Pawlowski et al. disclose wherein the processor has the lowest priority among one or more processors (see col. 4, lines 45-64).

In regard to claim 28, Pawlowski et al. disclose providing preferred ordering of the at least one updated TPR and at least one interrupt to be redirected (see col. 8, lines 22-37).

In regard to claim 60, Pawlowski et al. disclose redirecting at least one interrupt based on the task priority information (see col. 4, lines 45-64) and providing support for the updated TPR transactions to update at least one updated TPR register (see col. 9, lines 25-51).

Response to Amendment

12. Applicant's arguments with respect to claims 1-18 have been considered but claims 1-18 are deemed to be moot in view of the new grounds of rejection.

13. Applicant's arguments, see pages 13-14, filed June 25, 2003, with respect to the rejection(s)of claim(s) 1-18 under 35USC102 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Bennette and Pawlowski et al.

Conclusion

14. All claims are rejected.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Raymond Phan, whose telephone number is (703) 306-2756. The examiner can normally be reached on Monday-Friday from 6:30AM- 4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Primary, Paul Myers can be reached on (703) 305-9656 or via e-mail addressed to paul.myers@uspto.gov. The fax phone number for this Group is (703) 746-7239.

Communications via Internet e-mail regarding this application, other than those under 35 U.S.C. 132 or which otherwise require a signature, may be used by the applicant and should be addressed to **[raymond.phan@uspto.gov]**.

All Internet e-mail communications will be made of record in the application file. PTO employees do not engage in Internet communications where there exists a possibility that sensitive information could be identified or exchanged unless the record includes a properly signed express waiver of the confidentiality requirements of 35 U.S.C. 122. This is more clearly set forth in the Interim Internet Usage Policy published in the Official Gazette of the Patent and Trademark on February 25, 1997 at 1195 OG 89.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Paul R. Myers

PAUL R. MYERS
PRIMARY EXAMINER

Raymond Phan
9/7/03